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Design of 1-Bit SRAM Cell Using FinFET

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Abstract: CMOS technology shows certain limitations as the device is reduced more and more in the nanometre regime out of which power dissipation, current leakages, doping, and channel length is an important issue. FinFET is evolving to be a promising technology in this regard. In this project, designing, modelling and optimizing the 6-TSRAM cell device is done. Intrinsic variations and leakage control in today's world, is very difficult to achieve, So bulk-Si MOSFETs limit the scaling of SRAM. It is found that 6-T FinFET-based SRAM cells designed with built-in feedback achieve significant improvements in the cell static noise margin (SNM) without area penalty, read/write in time analysis. Improvement in SNM (signal to noise margin) can be achieved in 6-T FinFET-based SRAM cells. Improvements in SNM as the 6-T cell, making them attractive for low-power, low-voltage applications. The long-channel-device-based SRAM cell is marginally robust than optimized SRAM; however, increased gate-edge direct-tunnelling leakage and parasitic capacitances degrade the power consumption and access time.

Keywords: CMOS, 6-T SRAM, FinFET, Signal to noise margin, Simulation, Tanner.

I. INTRODUCTION

According to the Moore's Law, the number of transistors in a unit chip area double every two years. But the existing technology of integrated circuit formation is posing limitations to this law. CMOS technology shows certain limitations as the device is reduced more and more in the nanometre regime out of which power dissipation, current leakages, doping, channel length is an important issue. FinFET is evolving to be a promising technology in this regard. Inverter circuit is implemented in order to study the basic characteristics such as voltage transfer characteristics, leakage current and power dissipation. Further the efficiency of FinFET designed SRAM is increased, to reduce power as compared to CMOS using SRAM circuit. The predictive technology model (PTM) is used to simulate these CMOS and FinFET based SRAM which is a tentative model. Since the dimensions of the MOSFETs are deduced considerably, it is necessary to know the potential of both technologies, with its available least dimensions.

Now to solve the issues related to CMOS (such as SCE, Doping, NM, DIBL), specifically dealing with NM, Access time, Read/Write stability whichultimately increases efficiency in FinFET based design.This paper aims to analyse and compare the characteristics of CMOS and FinFET circuits at 45nm technology. The Predictive Technology Model is used to simulate this FinFET based SRAM which is a tentative model.

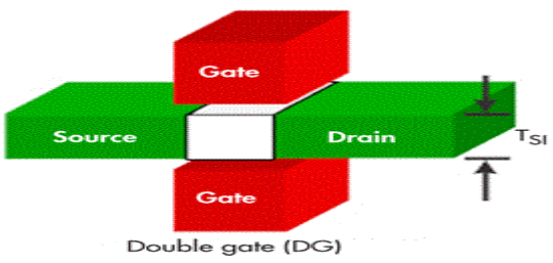

Fig.1 DG-FinFET

The quasi-planar double-gate FinFET has emerged as one of the most likely successors to the classical planar MOSFET for ultimate scalability. One of the leading replacement bulk and partially-depleted SOI CMOS due to its superior scalability for a given gate insulator thickness, better short-channel behaviour without complex channel engineering, higher mobility and the absence of random dopant fluctuation effects. The ideal MOSFET is essentially a gate-voltage controlled switch, and the short channel effect reflects the negative influence of drain-voltage on channel electrostatics as channel length decreases. The double-gate fully-depleted MOSFET diminishes the short-channel effect by bringing the gate closer to all regions of the channel, and thus improves scalability. The quasi-planar SOI FinFET and other variants have been proposed as easier manufacturable options compared to planar double-gate devices.

II. 6-T SRAM USING FINFET

Figure 2 shows the Schematic of 6T SRAM cell. This SRAM cell is composed of six transistor; four transistors (M1 – M4) comprise two cross coupled CMOS inverters plus two NMOS transistors (M5 and M6) for access.

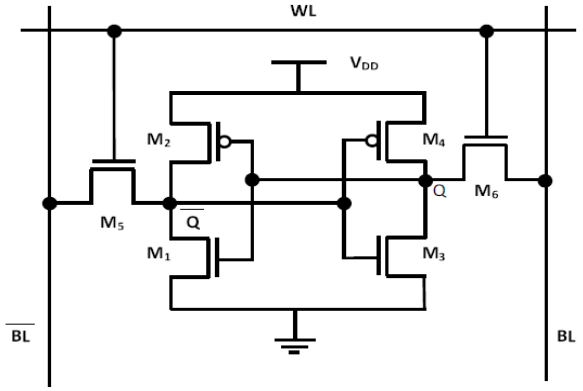

Fig 2 6-T Sram

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This configuration is called a 6T cell. Each bit in an SRAM is stored on four transistors that form two cross coupled inverters. This storage cell has two stable states which are used denote either 0 or 1. Two access transistors (M5 and M6) serve to control the access to a storage cell during read and write operations. Access to cell is enabled by the word line (WL) which controls the two access transistors which, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations.

A. Write Operation

Consider the write '0' operation assuming that logic '1' is stored in the SRAM cell initially. The voltage levels in the CMOS SRAM cell at the beginning of the data write operation. The transistors M1 and M6 are turned off, while M2 and M5 are operating in the linear mode. Thus the internal node voltage V1 = VDD and V2 = 0 before the access transistors are turned on.

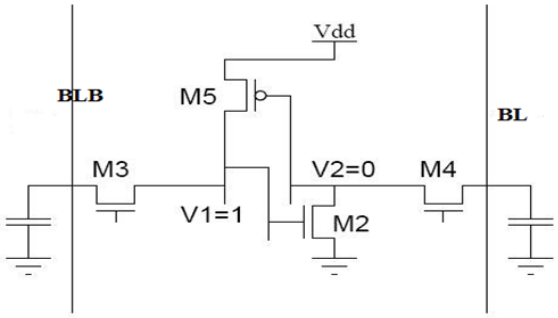

Fig 3.Writing Data

During write, VWL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, VWL is held low and the BLs are left floating or driven to VDD.

B. Read Operation

Consider a data read operation, assuming that logic '0' is stored in the cell. The transistors M2 and M5 are turned off, while the transistors M1 and M6 operate in linear mode.

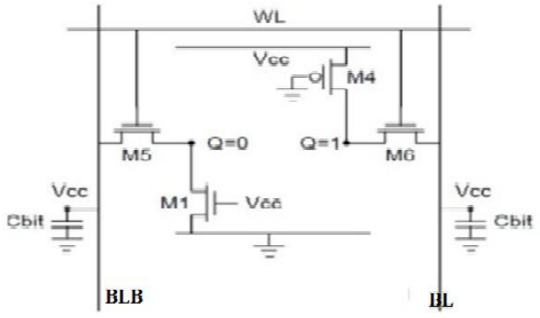

Fig 4.Reading Data

During read, the WL voltage VWL is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and QB. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail.

III.IMPLEMENTATION & RESULTS

To analyze the behaviour of Signal to Noise margin in 6-T SRAM, 7-T SRAM based FinFET design. Also comparing these results with CMOS.

A. 6-T SRAM using FinFET

VTC curve of a single inverter

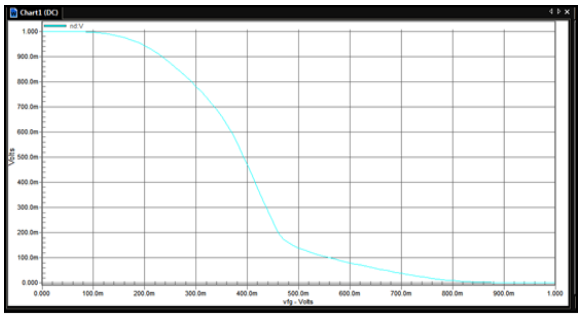

Fig 5.Inverter Output

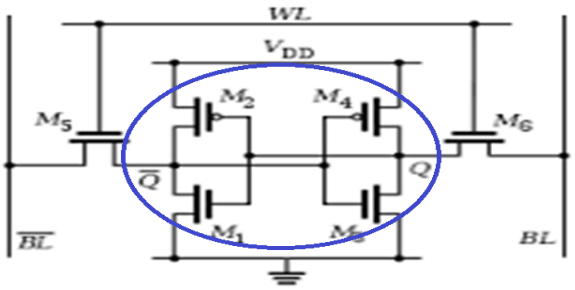

Fig 6.Back to Back inverter

PMOS:-W=60nm,L=45nm
NMOS:-W=60nm,L=45nm

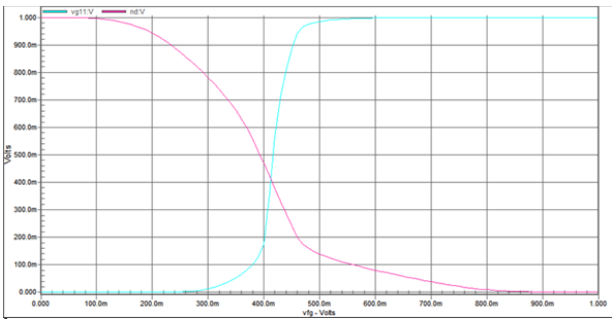

Fig 7.Butterfly curve

Testing inputs-DC input & DC WL-Writing BL=0, BLB=1

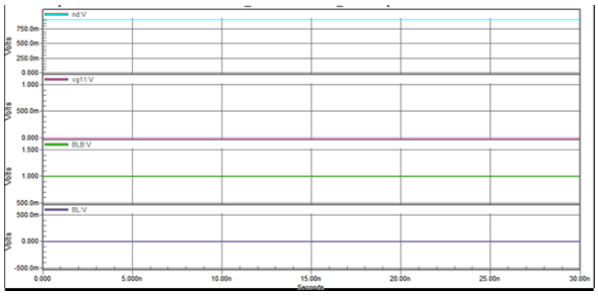

Fig 8.Write(BL=0,BLB=1)

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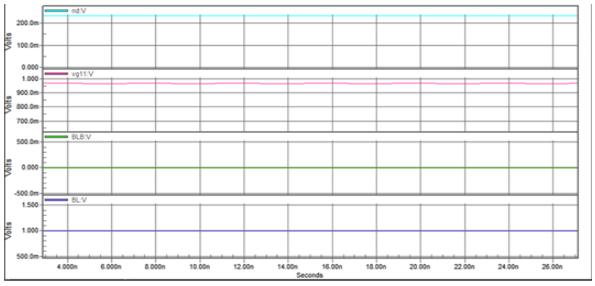

Fig 9.Write (BL=1,BLB=0)

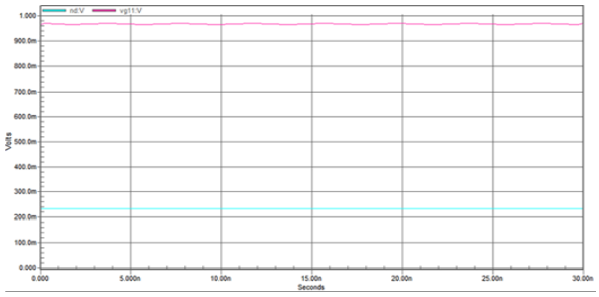

Fig 10. Read (vg11=1,nd=0)

Testing inputs-DC input & DC WL-Reading vg11=0, nd=1(As written values are BL=0, BLB=1)

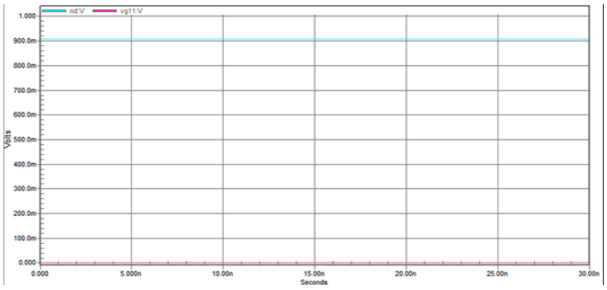

Fig 11.Read(vg11=0,nd=1)

DC input, Pulsed WL -Write BL=1,BLB=0

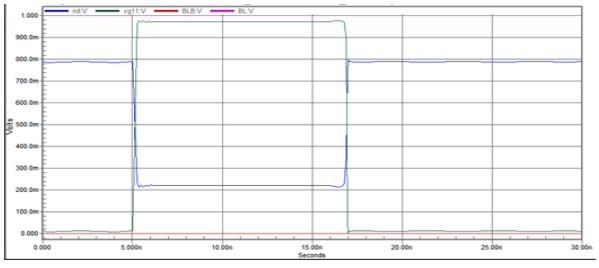

Fig 12.Write (BL=1)

DC input, Pulsed WL -Write BL=0, BLB=1

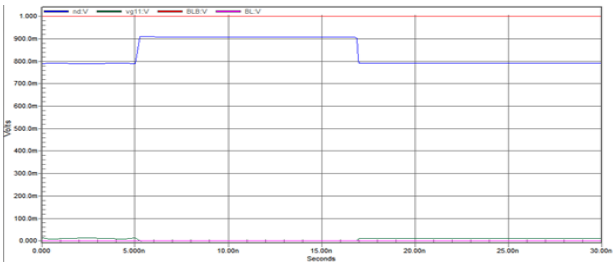

Fig 13.Write (BL=0)

Pulsed input, Pulsed WL -Write BL=1,BLB=0

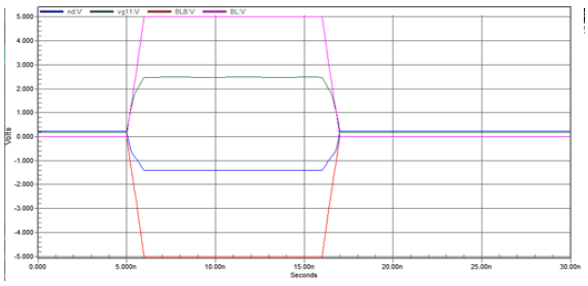

Fig 14.Write (BL=1)

Pulsed input, Pulsed WL -Write BL=0,BLB=1

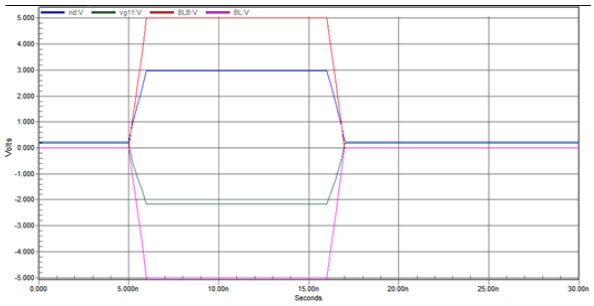

Fig 15.Write (BL=0)

Pulsed input, Pulsed WL –Read vg11=1, nd=0(As written values are BL=1,BLB=0) Now by changing W/L ratio(asymmatric)SNM has increased up by 1 unit.

Transistor	Width(W)	Length(L)
Access Transistor	80nm	45nm
Pull-up Transistor	50nm	45nm
Pull-down Transistor	280nm	45nm

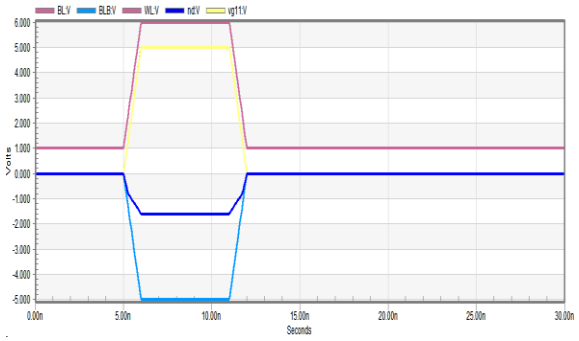

Fig 16.Write (BL=1)

B. 7-T SRAM using FinFET

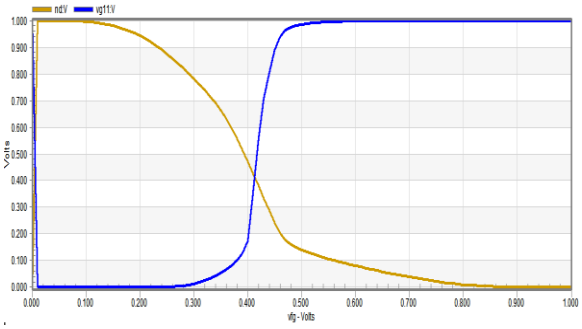

Fig17. Butterfly Structure

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Pulsed input, Pulsed WL-Write BL=1,BLB=0

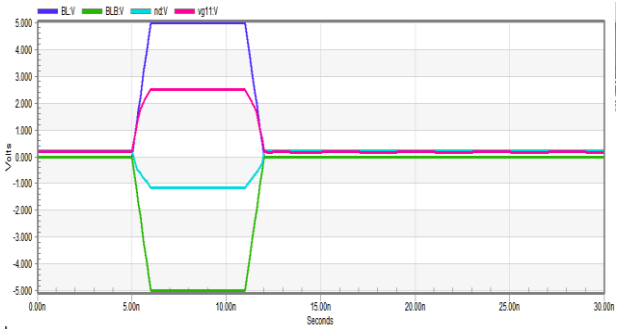

Fig 18.Write(BL=1)

Pulsed input, Pulsed WL-Write BL=0,BLB=1

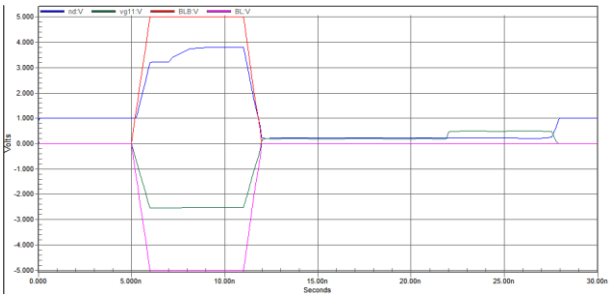

Fig 19.Write(BL=0)

Pulsed input, Pulsed WL–Read vg11=1v,nd=0v (As stored values are BL=1,BLB=0)

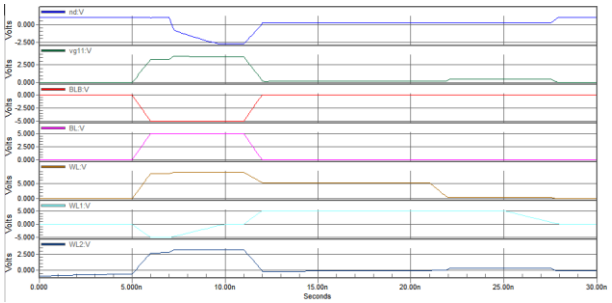

Fig 20. Read(BL=1)

Pulsed input, Pulsed WL–Read vg11=0v,nd=1v (As stored values are BL=0, BLB=1)

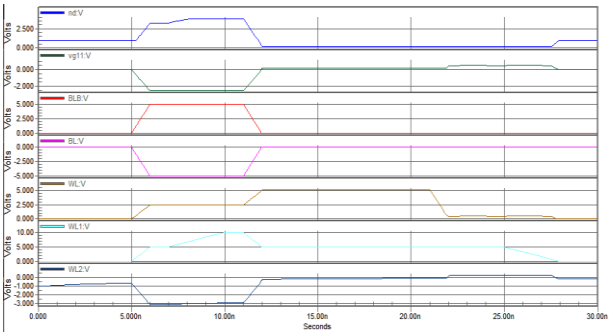

Fig 21.Read(BL=0)

Pulsed input, Pulsed WL –Read vg11=0v,nd=1v (As stored values are BL=0,BLB=1)

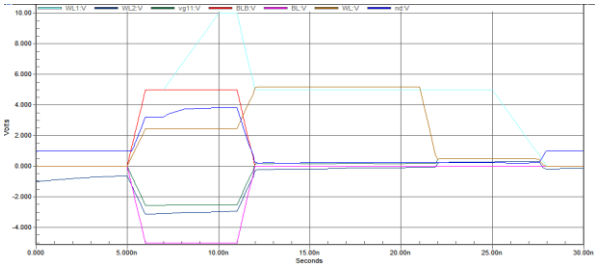

Fig 22.Read(BL=0)

C. 6-T SRAM using CMOS

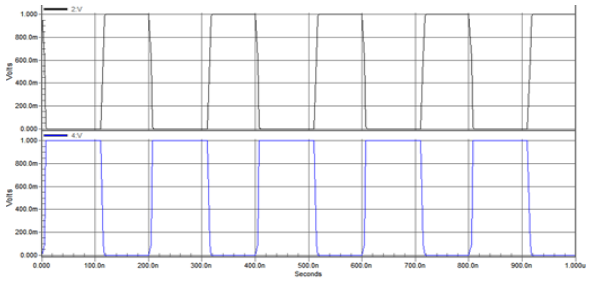

Fig 23.CMOS Inverter

DC input, DC WL -Write BL=0,BLB=1

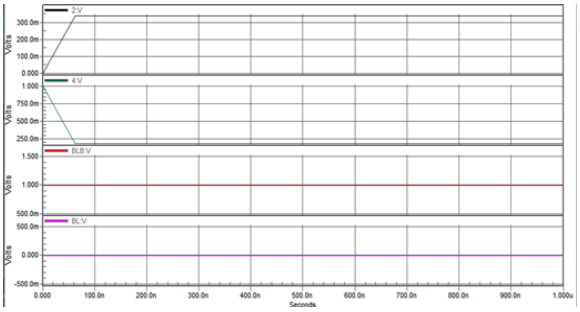

Fig 24.Write (BL=0)

DC input, DC WL -Write BL=1,BLB=0

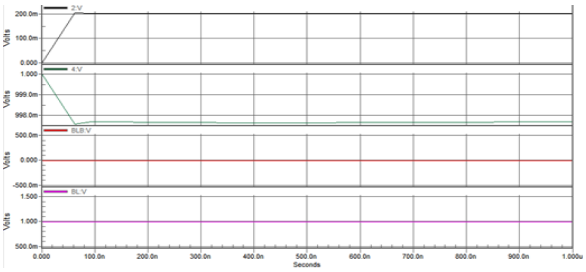

Fig 25.Write(BL=1)

DC input, DC WL–Read 2node=1v,4node=0v (As Stored values are BL=0,BLB=1)

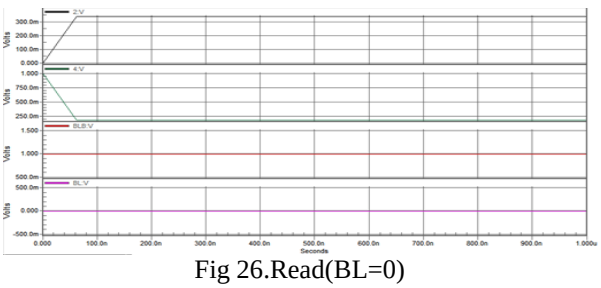

Fig 26.Read(BL=0)

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DC input, DC WL–Read 2node=0v,4node=1v (As Stored values are BL=1,BLB=0)

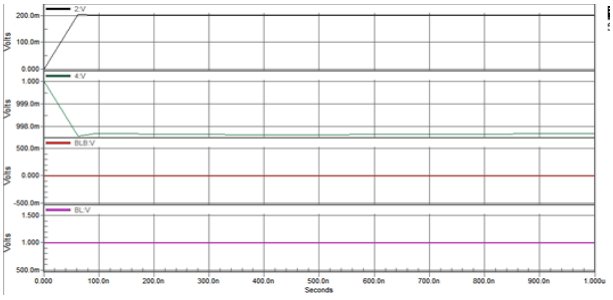

Fig 27.Read(BL=1)

Pulsed input, Pulsed WL -Write BL=0,BLB=1

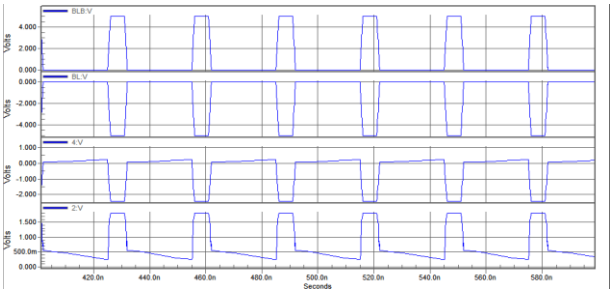

Fig 28.Write(BL=0)

Pulsed input,Pulsed WL -Write BL=1,BLB=0

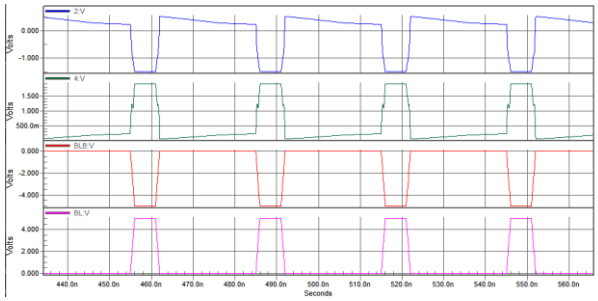

Fig 29.Write(BL=1)

DC input, Pulsed WL(denoted as node1) -Write BL=1,BLB=0

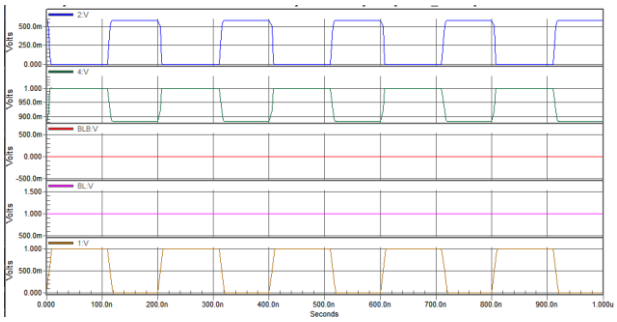

Fig 30.Write(BL=1)

Table 1.Comparative Analysis

Device/Parameters	6-T SRAM CMOS	6-T SRAM FinFET
SNM	Low	High

Table 2.Comparative size

Device /Parameter	6-T SRAM CMOS		6-T SRAM FinFET		7-T SRAM FinFET	
Vtn0	0.0259		0.0259		0.00259	
Vtp0	0.0259		0.0259		2.559	
	W	**L**	**W**	**L**	**W**	**L**
MN1	60nm	45 nm	280nm	45 nm	280 nm	45nm
MN2	60nm	45 nm	280nm	45 nm	280nm	45nm
MP1	60nm	45 nm	50 nm	45 nm	50nm	45nm
MP2	60nm	45 nm	50 nm	45 nm	50nm	45nm
MN3	60nm	45 nm	80 nm	45nm	80nm	45nm
MN4	60nm	40 nm	8nm	4nm	80nm	45nm
MN5	Absent		Absent		100 nm	45nm

IV. CONCLUSION

Based on above simulated results, I conclude that SRAM Finfet of 45nm technology has higher SNM ratio as compared to CMOS based SRAM. Also the read and write operation of 1 and 0 is performed and resulted correctly. The Data stored as per user requirement. Thus the analysis of read and write operation is performed perfectly. The higher SNM can be achieved by modifying the device parameters of conventional 6T SRAM cell without requiring any modification of the SRAM cell array design. Thus the analysis shows that 6T SRAM cell is more robust against process variation in terms of most of the design parameters compared to 7T SRAM cell.

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